ADVANCED PERFORMANCE, SECURITY, FUNCTIONAL SAFETY AND TIMER SYSTEMS FOR ENGINE/INDUSTRIAL APPLICATIONS

MPC5777C

30, MARCH, 2016
Engine Control MCU Market Trends

Exponential MCU performance demands
• Need 3-5x increase in performance to support software and emission filtering

Increased memory requirements
• Support of large legacy code and increased use of auto coding driving the need for larger memory sizes

Emerging safety and security standards
• Enable ASIL-C or ASIL-D functional safety
• Tamper detection modules and hardware encryption capabilities to deter code tampering and enable secure communication

Lower Power
• Power targets at 60% of previous generation MCUs
• Increase in multi-core processing to enable current consumption reduction and simultaneous performance increase
Introducing the **New** Qorivva MPC5777C Multicore MCU

**Performance, Security, Timer System, Functional Safety**

**Performance & Architecture Efficiency**
High performance (264MHz), multi-core (3 z7 cores, 2 in Lock Step with each other) Power Architecture based platform

**Security**
Cryptographic Services Engine (CSE), provides a hardware security module with encryption/decryption capabilities and secure key storage

**Timer System**
Industry standard eTPU timer system for advanced timing requirements

**Functional Safety**
Enables highest level of functional safety (ASIL-D) support
Target Engine Applications for MPC5777C Family

- 2-4 Cylinder Engine Management
- Transmission
- 6 Cylinder Engine Management
- HV/EV Management
- 8+ Cylinder Engine Management

MPC5777C
8 MB Flash
512 kB SRAM

416/516 MAPBGA
NXP Automotive Powertrain MCU Products

**MPC55XX**
- 130nm
- 32-bit MCU
- 2 MB Flash
- 132MHz
- 32-bit MCU targeted for Engine Management
- Mid 2000s

**MPC56XX**
- 90nm
- 32-bit MCU
- 4 MB Flash
- 264MHz
- Setting the Performance Standard for the industry
- Production Now

**MPC5777C**
- 55nm
- 32-bit MCU
- 8 MB Flash
- 2x264MHz Cores
- Lock Step Core
- Multicore with Safety and Security
- Production 2016
Powertrain MCU Portfolio

**Applications**
- **High-end**
  - >6 Cylinder
  - MPC556x
- **Mid-range**
  - 6 Cylinder Transmission HEV / EV
  - MPC556x
  - MPC567xR
    - 2 x 180 MHz
    - 6M, eTPU2
  - MPC567xF
    - 264 MHz
    - 3M – 4M, eTPU2
  - MPC564xA
    - 150 MHz
    - 2M – 4M, eTPU2
  - MPC563xM
    - 80 MHz
    - 768K – 1.5M, eTPU2
- **Low-end**
  - <= 4 Cylinder
  - S12 (X)

**2016**
- MPC5777M
  - 2 CC at 300 MHz
  - 1 LS at 300 MHz
  - 1 IOP at 200 MHz
  - 8M, GTM
- MPC5777C
  - 2 CC at 264 MHz
  - 1 LS at 264 MHz
  - 8M, ETPU
- MPC5746R
  - 2 CC at 200 MHz
  - 1 LS at 200 MHz
  - 4M, ETPU

**< 2011**
- MPC556x
- MPC567xR
  - 2 x 180 MHz
  - 6M, eTPU2
- MPC567xF
  - 264 MHz
  - 3M – 4M, eTPU2
- MPC564xA
  - 150 MHz
  - 2M – 4M, eTPU2
- MPC563xM
  - 80 MHz
  - 768K – 1.5M, eTPU2

**Sampling**
- Single Core
- Dual Core
- Multi Core

**Production**
- CC – Computation core
- IOP – I/O processor
- LS – Lockstep core
- GTM – General Timer Module
- ETPU – ETPU Timer Module
MPC5777C Advanced Architecture

**Multicore Processing**  
(enhances throughput)

**Lockstep Core**  
(safety)

**Local I-RAM / D-RAM**  
(instruction RAM, data RAM)  
to maximize throughput

**Crossbar**  
(reduces delays in multicore memory access)

**Embedded Flash / RAM**

**Crossbar Switch with ECC – 132MHz**

**Broad Communication Peripherals**  
(Ethernet, CAN, LIN, etc)

- **eTPU+ (A + B)**
- **16ch eMOS**
- **1 x eQADC**
- **2 x SD ADC**
- **2 x STIx**
- **CMU + PMU**
- **PIT / RTI**
- **SENT**
- **FCCU**

**High-Speed A/D Converters**

**CAN FD**  
(2 MCAN modules with ISO Compliant CAN FD)

**eTPU**  
(advanced timer)
**Cores & Memory**
- Two independent z7 dual issue computational cores @ 264MHz
  - Cores include VLE, SPE1.1, FPU, MMU
  - 16kB L-cache & 16kB data-cache w/coherency
- Single z7 lockstep core @ 264MHz (for ISO26262 and ASIL-D)
- Up to 8.25MB Flash RWW w/ECC including 4x64kB EEPROM
- Up to 589kB total SRAM
  - 512kB on chip static RAM w/ECC (up to 48kB standby)
  - 45kB eTPU RAM, 32kB data cache (w/line locking)
- Security
  - PASS and TDM (Tamper Detection)
  - CSE2 (Crypto Services Engine for Encryption & Secure Boot)

**I/O & System**
- Up to 70ch eQADC from 4 converters w/12bit resolution
  - On-chip temperature sensor and VGA (x1,x2,x4)
  - 12 x Decimation Filters w/hardware knock integrators
  - 20ch ΣΔ ADC (4 converters w/16bit resolution)
  - Timers – up to 128 channels (96ch eTPU2+ and 32ch eMIOS)
  - 2 x 64ch eDMA support (128ch total)
  - 6 x CAN ports (4 x FlexCAN + 2 x MCAN)
  - Ethernet
  - DSPI – 5 channels (2 supporting µSec ch.)
  - eSCI – 6 channels (2 supporting uSec ch.)
  - Reaction module – 10 channels for current control
  - Up to 12ch SENT, Zipwire, 2ch PSI-5
  - 1 x CRC unit – w/3 independent channels,
  - 4 x protected port outputs, MPU and MMU
  - FMPLL + PLL
  - Safety Monitors – e2eECC, CLK, Voltage, Fault Collection

**Packaging & Enablement**
- 416 MAPBGA, 516 MAPBGA
- Calibration – VertiCal (using 552CSP)
# MPC5777C Feature Set

<table>
<thead>
<tr>
<th>Feature</th>
<th>Specification</th>
<th>MPC5777C</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>CPU</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Clock</td>
<td>MHz</td>
<td>264</td>
</tr>
<tr>
<td>Main core number</td>
<td></td>
<td>2</td>
</tr>
<tr>
<td>Locked step core number</td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>I-Cache KB/core</td>
<td></td>
<td>16</td>
</tr>
<tr>
<td>D-Cache KB/core</td>
<td></td>
<td>16</td>
</tr>
<tr>
<td><strong>Flash</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Code flash KB</td>
<td></td>
<td>8,000</td>
</tr>
<tr>
<td>Data flash KB</td>
<td></td>
<td>264</td>
</tr>
<tr>
<td><strong>RAM</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Total System RAM KB</td>
<td></td>
<td>512</td>
</tr>
<tr>
<td>Standby RAM KB</td>
<td></td>
<td>64</td>
</tr>
<tr>
<td><strong>Complex Timer</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>eTPU mod/ch</td>
<td></td>
<td>3/96 Total</td>
</tr>
<tr>
<td>eMIOS mod/ch</td>
<td></td>
<td>2/32</td>
</tr>
<tr>
<td>Reaction Module ch</td>
<td></td>
<td>10</td>
</tr>
<tr>
<td><strong>LINFlex (UART)</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DSPI ch</td>
<td></td>
<td>5</td>
</tr>
<tr>
<td>SENT ch</td>
<td></td>
<td>12</td>
</tr>
<tr>
<td><strong>CAN</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CAN2.0 mod</td>
<td></td>
<td>6 (2 with ISO Compliant CAN FD)</td>
</tr>
<tr>
<td>eQADC mod/ch</td>
<td></td>
<td>4/70 Total</td>
</tr>
<tr>
<td>SD ADC mod/ch</td>
<td></td>
<td>4</td>
</tr>
<tr>
<td>DECIMATION FILTER mod</td>
<td></td>
<td>12</td>
</tr>
<tr>
<td>PKG</td>
<td></td>
<td>MAPBGA416/516</td>
</tr>
</tbody>
</table>
MPC5777C Flash Partitioning

- Four 1 x 64K partitions
  - Data Segment (EEPROM)
- Four 8 x 256K partitions
  - 1 x 256K block for Boot
  - 4 x 256K blocks for Calibration
  - 27 x 256K blocks for Code
- Split memory address ranges:
  - 0x00000000 to 0x0003FFFF
  - 0x00800000 to 0x00FFFFFF
- Expanded Data Segment address range

<table>
<thead>
<tr>
<th>Addr</th>
<th>Size</th>
<th>Example Usage</th>
</tr>
</thead>
<tbody>
<tr>
<td>000000 – 00FFFF</td>
<td>64K</td>
<td>EEPROM/Data</td>
</tr>
<tr>
<td>010000 – 01FFFF</td>
<td>64K</td>
<td>EEPROM/Data</td>
</tr>
<tr>
<td>020000 – 02FFFF</td>
<td>64K</td>
<td>EEPROM/Data</td>
</tr>
<tr>
<td>030000 – 03FFFF</td>
<td>64K</td>
<td>EEPROM/Data</td>
</tr>
<tr>
<td>...</td>
<td></td>
<td>...</td>
</tr>
<tr>
<td>800000 – 83FFFF</td>
<td>256K</td>
<td>Boot (256K)</td>
</tr>
<tr>
<td>840000 – 87FFFF</td>
<td>256K</td>
<td>Calibration (1024K)</td>
</tr>
<tr>
<td>880000 – 8BFFFF</td>
<td>256K</td>
<td></td>
</tr>
<tr>
<td>8C0000 – 8FFFF</td>
<td>256K</td>
<td></td>
</tr>
<tr>
<td>900000 – 93FFFF</td>
<td>256K</td>
<td></td>
</tr>
<tr>
<td>940000 – 97FFFF</td>
<td>256K</td>
<td>Appl Code (4864K)</td>
</tr>
<tr>
<td>...</td>
<td></td>
<td>...</td>
</tr>
<tr>
<td>B80000 - BBFFFF</td>
<td>256K</td>
<td></td>
</tr>
<tr>
<td>BC0000 - BFFFF</td>
<td>256K</td>
<td></td>
</tr>
<tr>
<td>C0000 – C3FFFF</td>
<td>256K</td>
<td></td>
</tr>
<tr>
<td>C4000 – C7FFFF</td>
<td>256K</td>
<td></td>
</tr>
<tr>
<td>...</td>
<td></td>
<td>...</td>
</tr>
<tr>
<td>D80000 - DBFFFF</td>
<td>256K</td>
<td></td>
</tr>
<tr>
<td>DC0000 - DFFFFF</td>
<td>256K</td>
<td></td>
</tr>
<tr>
<td>E00000 – E3FFFF</td>
<td>256K</td>
<td></td>
</tr>
<tr>
<td>E40000 – E7FFFF</td>
<td>256K</td>
<td></td>
</tr>
<tr>
<td>...</td>
<td></td>
<td>...</td>
</tr>
<tr>
<td>F80000 - FBFFFF</td>
<td>256K</td>
<td></td>
</tr>
<tr>
<td>FC0000 - FFFFFF</td>
<td>256K</td>
<td></td>
</tr>
</tbody>
</table>
MPC5777C Security

- Hardware block to manage Lifecycle Security State
  - e.g. Out of Fab, Customer Delivery, OEM Development, In-Field, Failure Analysis
  - Updates to Lifecycle Security State are password protected
- Secure Password Storage and Management
  - Secure Flash Blocks, CSE2 security module
- Password protected configuration of Flash Access Rights
  - Read access, Erase/Program Controls
- Flash Tamper Detection
  - Irrevocably logs flash reprogram attempts
- Password protected JTAG access
- Supports Root of Trust through Secure Boot hardware
  - AES-128 CMAC
- Supports Global B Architecture for Security Key Management
  - AES-128 CMAC Generation/Verification, Encryption/Decryption
eTPU Features

- Powerful Channel Hardware
- FAST Optimized Microengine
- Angle Clock Hardware
- 24-bit Compare and Match
- Very Low Latency (6 clocks)
- Independent Code and Data Store
- Autonomous from Host CPU
- 33 Interrupt Sources
- DMA Client
- Nexus III Debug Interface
- State-of-the-Art Tools
- Unequaled I/O Control Performance
MPC5777C Analog Converter – Sigma Delta ADC

- The SDADC consists of a cascaded sigma delta modulator coupled to a high pass filter and digital interface to the system bus. Both single ended and differential conversions are supported on a number of input channels. Conversions can be started by software or hardware triggers.
  - 16-bit data resolution output
  - Single-ended input or differential input mode of operation
  - Configurable biasing for negative input terminal in single-ended mode
  - Gain and offset calibration support using fixed bias for input terminals
  - Programmable decimation rate and programmable gain for analog inputs
  - Optional external modulator support and optional high-pass filter for pure AC application
  - Hardware trigger support for synchronous operation of multiple SDADC blocks
  - Trigger event output generation by software
  - Programmable FIFO structure for storing 16-bit converted data
  - Left/right data alignment
  - Signed/unsigned format of converted data output
  - Programmable threshold range WatchDog (WDG) support
  - Interrupt/DMA request generation based on various conditions:
    - Data buffer at or above threshold
    - Data buffer overrun
    - WDG crossover event
MPC5777C Reaction Module

- Provides autonomous closed loop control of transmission valves and other inductive loads
- Supports Peak and Hold PWM current levels
- Two PWM modes supported
- Configurable hardware interfaces to eQADC and eTPU
- 10 independent channels
- Up to 3 output drive signals per channel
- Programmable hardware state machine controls sequencing of output drives
- Open and short circuit detection in hardware
MPC5777C Zipwire

- Zipwire is the combination of the SIPI application layer protocol and LFAST physical layer.
  - SIPI is a bus master that accesses the shared memory assigned to a remote device
  - LFAST is the asynchronous 320Mbps LVDS interface
- Full duplex 4 channel communication
- DMA access
- CRC protection mechanism
- Timeout protection mechanism
- Up to 256 bits on one streaming channel
MPC5777C SENT

- Multi-channel receiver for sensor data
- Separate buffers for Fast and Slow Serial Messages
- Separate DMA and Interrupts generated for Fast and Slow Serial Messages
- Implements diagnostics as specified by the SAE
MPC5777C PSI5

- A high-speed and high-reliability data transfer interface for automotive sensor applications
- Only speed of 125 Kbit/s supported
- Two-wire current interface
- Time triggered options
MPC5777C Ethernet

- The Fast Ethernet Controller (FEC) is a communication controller that supports 10 and 100 Mbps Ethernet/IEEE 802.3 networks
- External PHY transceiver required
- Supports Media Independent Interfaces: MII-Lite and RMII.
MPC5777C Safety Concept

• Part of NXP’s “SafeAssure” functional safety program to ease the process of achieving functional safety standards in the automotive and industrial markets.

• The SafeAssure solutions reduce the time it takes to develop safety systems that comply with the International Standards Organization (ISO) 26262 and International Electrotechnical Commission (IEC) 61508 standard safety measures.

• Based on Defined Safety Goals

• Measures to detect single point faults
  - Replication of Cores
  - End-2-End protection of data paths
  - ECC on all RAMs (System, periphery, Cache, TCM) & Flash

• Measures to detect latent errors (during boot)
  - Memory BIST (MBIST)
  - LBIST
  - Limited BIST of analog components

• Measures to detect Common Cause errors
  - Clock & Power Monitors
  - Temperature Sensors
  - I/O channels split between two bridges and physically separated on SoC

• Fault collection and reporting managed by a fault control and collection unit (FCCU)

• A “Safe State” for the chip is defined
  - entered when specified fault conditions occur

• SoC is developed in compliance with ISO 26262 ASIL D level
  - Includes requirements and definition management, FMEDA analysis
MPC5777C Calibration & Debug Strategy

• MPC5777C uses same VertiCal calibration system as older generation MPC5676R

• Supports the same debug features as MPC5676R with additional features:
  – Adds IEEE1149.7 support
  – Adds trace client for Zipwire
  – Adds JTAG Data Communications (JDC) module
MPC5777C JTAG Data Communication (JDC)

- JDC has JTAG Interface & Software Interface
- 32 bit Input Register and 32 bit Output Register
- Includes flag/interrupt bits for input and output to help manage flow control between JTAG & software
- JDC is always accessible, even when JTAG Debug is disabled (e.g. When censored)
- The JDC provides a software method of enabling debug access using application code protocol (e.g. challenge/response)
MPC5777C Family Enablement

• Compilers
  • Green Hills
  • Wind River

• Debuggers
  • Lauterbach
  • iSystem
  • P&E
  • PLS

• HW Development Boards
  • Motherboard MPC57XXXMB $439
  • Daughterboards:
    • 416 BGA MPC5777C-416DS $295
    • 516 BGA MPC5777C-516DS $395

• VertiCal Calibration Boards
MPC5777C Family Summary

• High performance
  • Multicore, Power Architecture 264MHz z7 cores
  • 8M Flash

• Security
  • Cryptographic Services Engine (CSE) provides a hardware security module with encryption/decryption capabilities and secure key storage

• Timer System
  • Industry standard eTPU timer system for advanced timing requirements

• Functional Safety
  • Supports ASIL-D applications